AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

~~Claims:~~**We Claim**

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1. (Currently amended) A method of monitoring a reduction in thickness of a bonded **pair of** semiconductor ~~wafer pair comprised of~~**wafers, having** a first and a second wafer (~~1, 2~~**1,2**), the method comprising

- forming a test structure ~~(4,5,6,7,8,9), defined by~~**having** a systematic row of ~~a plurality of~~**trenches in an active wafer, said** trenches having different **defined** widths ~~in a defined manner, in an (active) wafer (2),~~ said **active** wafer **provided for** receiving an active circuit in a later ~~stage;~~**step;**

~~wherein a targeted thickness (h6;h7) of the active wafer (2) during the removal corresponds to a depth (t6;t7) of a reference trench (6;7) of the trenches of the test structure, said reference trench (6) being flanked by shallower and deeper trenches, in particular by a neighbouring shallower and a neighbouring deeper trench (5,7);~~

- bonding the active wafer ~~(2)~~ with a side ~~(2a), in~~ which **holds** the test structure ~~is formed,~~ onto the second wafer of the semiconductor wafer pair~~, in particular onto a carrier wafer (1)~~;

- wherein a targeted thickness of the active wafer during a removal corresponds to a depth of a reference trench of the row of trenches in said test structure, said reference trench neighboured by a shallower and a deeper trench;

- performing a**the wafer** material removal process~~, in particular~~ **comprising** a polishing process, **commencing** from the**a** backside of the **bonded** active wafer ~~(2)~~ until the reference trench ~~(6)~~ is exposed, ~~which is optically detectable and is~~**and** optically detected,

~~respectively~~ for monitoring ~~the~~**a thickness** reduction ~~in thickness~~ of the ~~first wafer (2).~~**active wafer; and**

- **forming an active circuit in said active wafer in said later step.**

2. (Currently amended) The method of claim 1, wherein the systematic row comprises ~~tenches (4 to 9)~~**trenches** of different depths.

3. (Currently amended) The method of claim 2, wherein ~~the~~ deep trenches are formed in an etch process using an etch mask having openings of different widths for the trenches of different widths~~, in particular prior to bonding the active wafer (2) onto the carrier wafer (1)~~.

4. (Currently amended) The method of claim 1, wherein the trenches ~~(4 to 9)~~ are not filled~~, that is, are~~ **or** unfilled ~~or open,~~ prior to bonding the active wafer ~~(2)~~**to the second wafer**.

5. (Currently amended) The method of claim ~~1~~**1,** wherein the active wafer ~~(2)~~ is a wafer formed of a semiconductor crystal~~, in particular formed of silicon~~.

6. (Currently amended) The method of claim 1, wherein the ~~carrier~~**second** wafer ~~(1)~~ at least comprises an insulating layer~~, in particular formed of silicon dioxide~~.

7. (Currently amended) The method of claim 1, wherein the systematic row is a sequence of trenches~~, in particular parallel trenches,~~ that become continuously shallower or continuously deeper.

8. (Currently amended) The method of claim 1 or 7, wherein the trenches are formed as stripe-like trenches **each having a certain depth and width**, and wherein ~~the~~**a** respective ~~depths increase~~**depth increases** as the ~~widths increase~~**corresponding width increases**.

9. (Currently amended) The method of claim 1, wherein prior to reaching ~~the~~**a** bottom ~~(6a)~~ of the reference trench~~, that is,~~ **by the removal process, and** prior to exposing the ~~bottom of the~~

reference trench ~~(6)~~, the removal ~~10~~ process is interrupted at least once for **one of an** optical monitoring ~~or~~**and** observation ~~(30)~~.

10. (Currently amended) A device for monitoring a reduction in thickness of a bonded semiconductor wafer pair comprised of a first and a second wafer ~~(1,2)~~, **the device** comprising

- a test structure ~~(4,5,6,7,8,9)~~ of a systematic row of a plurality of trenches having different widths in a defined manner and formed in the first wafer ~~(2)~~, said first wafer ~~for receiving~~**comprising** an active circuit ~~in a later stage~~, wherein

~~a targeted thickness (h7) of the active wafer (2) during the removal corresponds to a depth (t7) of a reference trench (7) of the test structure;~~

- said active wafer ~~(2)~~ is bonded with a side ~~(2a)~~, in which the test structure is or was formed, onto the second wafer of the semiconductor wafer pair~~, in particular onto a carrier wafer (1);~~

~~for performing a material removal process, in particular a polishing process,~~ **a thickness of the active wafer corresponds to a depth of a reference trench of the test structure as targeted thickness during a removal process** from the backside of the active wafer ~~(2)~~ until the reference trench ~~(71, in particular~~**and** the bottom ~~(7a)~~ of the reference trench~~, is~~ **was** exposed~~; and an optical device (30) for monitoring the reduction in thickness~~.

11. (Currently amended) The device of claim 10, wherein the trenches ~~(4 to 9)~~ are not filled with a fill material.

12. (Currently amended) The device of claim 10, wherein systematic row of trenches of different depths ~~also~~ comprises a systematic configuration with respect to the widths of the trenches such that the trenches are broader the more deeply they are formed in the first **as active** wafer.

13. (Currently amended) The ~~device of claim 10 or the~~ method of claim 1, wherein the targeted thickness is the desired or **a** predefined target thickness.

14. (Currently amended) The method of claim 9 or 1, wherein the removal process~~, in particular~~ **comprising** the polishing process~~.~~ **is** performed from the backside~~,~~ **and** is terminated when an optical observation ~~(30)~~ reveals exposure of **a bottom of** the reference trench ~~(6), that is exposure is detectable by the~~**, an** optical device ~~from~~**is directed towards** the backside of the active wafer ~~(2)~~**fore such optical observation**.

15. (Currently amended) The device of claim ~~10 or the method of claim 1,~~**10,** wherein the reference trench ~~(6;7)~~ is located in a central region of the systematic row and on one side of the reference trench ~~is located~~ at least one or more trenches of smaller depth **are located,** and at the other side of the reference trench ~~is located at least~~ one or more trenches of greater depth~~.~~ **are located.**

16. (Currently amended) The device ~~or method~~ of claim 15, wherein on one side ~~is located~~ at least one or more trenches of smaller width and on the other side ~~is located~~ at least one or ~~I~~ more trenches of greater width **are located**.

17. (New) The method of claim 1, wherein the second wafer is a carrier wafer.

18. (New) The method of claim 1, wherein the row of trenches comprising a plurality of parallel trenches, each having a different width.

19. (New) The method of claim 1, wherein the neighbouring trenches are several deeper and several shallower trenches.

20. (New) Method of claim 3, wherein the etch process is performed in particular prior to bonding the active wafer onto the second wafer as carrier wafer.

21. (New) Method of claim 4, the not filled trenches being open prior to said bonding.

22. (New) Method of claim 5, the active wafer is comprised of silicon.

23. (New) Method of claim 6, the second wafer as carrier wafer comprises the insulating layer formed of silicon dioxide.